

3D Semicircular Flash Memory Cell: Novel Split-Gate Technology to Boost Bit Density

M. Fujiwara, T. Morooka, S. Nagashima, T. Kato, N. Fukuda, N. Kariya, T. Ogura, T. Kurusu, Y. Shimada, T. Ishikawa, Y. Arayashiki, K. Hirayama, Y. Koyama, S. Kashiyama, W. Cai, Y. Goki, K. Sawa, D. Ikeno, M. Nishikawa*, Y. Uchiyama, N. Ohtani, F. Arai, and M. Kondo
Kioxia Corporation, Yokkaichi, Mie, Japan, *Western Digital Corporation, Yokkaichi, Mie, Japan
Email: makoto.fujiwara@kioxia.com

Abstract—Three-dimensional (3D) semicircular split-gate flash memory cells have been successfully developed for the first time. Reduction of fringing field effects is essential to extract maximum performance from the split-gate cells, and careful design of Floating Gate (FG) cells achieves superior program slope and program/erase window at much smaller cell size relative to circular Charge Trap (CT) cells. It is projected that the semicircular split-gate FG cell is a promising candidate to realize more than four bits/cell (QLC) for significantly higher memory density at a lower number of stacking layers.

I. INTRODUCTION

3D flash memory technology has realized high bit density with low cost per bit by increasing the number of cell stacks and implementing multilayer stack deposition and high aspect ratio etch [1]. In recent years, as the number of cell layers is exceeding 100 [2], managing the fundamental trade-offs among etch profile control, size uniformity and productivity is becoming increasingly challenging. In order to continuously attain higher bit density, cell size reduction is a viable approach. As shown in Fig. 1, smaller cell size allows for higher-density memories at the lower number of cell layers that can improve process control and reduce cost of the multilayer film deposition and etch. Meanwhile, simple reduction of cell size leads to larger characteristics variations and higher random telegraph noise [3], where smaller ISPP (Incremental Step Pulse Programming) steps must be applied to ensure sufficient program/erase window, causing the substantial reduction in program speed (Fig. 2). It is evident that increasing average program slope of small-size cells, thus suppressing program disturb to enlarge program/erase window [4], is critical to achieving comparable program speed to larger cells. This work reports the first demonstration of the 3D semicircular split-gate cell technology that realizes a considerable reduction in cell size compared to the conventional circular cell. The main physical mechanisms affecting split-gate cell characteristics are addressed, providing a systematic comparison between 3D CT and 3D FG devices in terms of program/erase characteristics and reliability.

II. SELECTION OF CONTROL-GATE SHAPE

The shape of the Control Gate (CG) plays an important role for the program/erase characteristics and reliability, and two different designs, circle and flat [5], have been employed in 3D

flash memory cells. Fig. 3 compares simulated program window and program saturation between the circle and the flat types. The circle-shaped control gate provides larger program window with relaxed saturation problems because of the curvature effect [6], where carrier injection through the tunnel dielectric is enhanced while electron leakage to the block dielectric is lowered. In this split-gate cell design, the circular control gate is symmetrically divided into two semicircular gates to take advantage of the strong improvement in the program/erase dynamics.

III. SEMICIRCULAR CHARGE TRAP CELLS

A. Cell Structure and Process Flow

Fig. 4 illustrates the schematic cell structures of the split-gate CT cells. The control gates of facing cells are separated by trenches filled with SiO₂, and cell stack films consisting of block (BLK), charge trap (CT), tunnel (TNL) and channel are formed inside the ellipsoidal holes extending over the trenches.

Major process flow for the semicircular CT cell fabrication is depicted in Fig. 5. After deposition of multilayers of SiO₂ and sacrificial SiN, cell isolation trenches are etched and filled with SiO₂. Then, the ellipsoidal memory holes are formed on the trenches, followed by formation of the cell stack films. The sacrificial SiN is stripped and replaced by CG metal. Fig. 6 shows the TEM cross-section and plane view of the semicircular CT cells that are electrically evaluated.

B. Cell Characteristics

Fig. 7 compares program/erase characteristics between the fabricated semicircular and circular cells. It is obvious that the average program slope of the semicircular CT cell is considerably decreased to 0.37 V/V when compared with 0.83 V/V of the circular CT cell. In order to examine the main cause for the program slope degradation, TCAD simulations with calibrated parameters were performed. As shown in Fig. 8, simulated results are in good agreement with the experimental characteristics, and systematic analyses clearly identify that the major factors for the program slope reduction are the fringing field effects attributed to parasitic leakage paths at the CG edge regions before the main channel turns on.

This parasitic effects can be mitigated by introducing highly localized electron injection into the CG edge areas to suppress the edge turn-on. In the initial charge injection technique, described in Fig. 9, high positive voltage is applied to both of facing cells to inject electrons, followed by hole injection at

relatively low voltage so that electrons or negative charges remain locally at the CG edges of the CT. Experimental results in Fig. 10 confirm that the local modulation of charge distribution to raise V_t at the parasitic CG edges indeed increases the program slope. However, the program slope of the semicircular CT cell is still lower than the value of the circular cell owing to the residual fringing field effects, which considerably deteriorates program speed at reduced cell size.

IV. SEMICIRCULAR FLOATING GATE CELLS

A. Cell Structure and Process Flow

In order to further increase the program slope of the split-gate cells, the conductive storage layer consisting of poly-Si has been extensively investigated, aimed at higher charge trapping efficiency relative to the dielectric storage layer (CT). Fig. 11 shows the schematics of the cross-section and plane view of the semicircular split-gate FG cells. Unlike the 3D CT cells, where the CT is connected from top to bottom cells, the FG is completely isolated for each cell, which eliminates charge migration across adjacent cells. In addition, the conductive storage layers placed between the CG and the channel act as electric field shields, hence mitigating the parasitic turn-on at the semicircular gate edges.

Process flow used to fabricate the semicircular FG cell is described in Fig. 12. After multilayer deposition of SiO and sacrificial SiN, cell isolation trenches are formed by dry etch process and filled with SiO. Memory holes are formed in the trenches, and then the sacrificial SiN is partially etched. BLK and FG of cell stack films are formed inside the memory holes and recessed back to isolate the FG for each cell. Then, TNL and channel are formed, followed by removal of the sacrificial SiN and subsequent CG metal replacement. Fig. 13 shows the TEM cross-section and plane view of the semicircular FG cells. The channel Si and TNL are surrounded by the semicircular FG and BLK that are separated from adjacent cells.

B. Cell Characteristics

Design optimization of the distance between the CG and the channel along with the electric field shielding effect of the FG drastically attenuate the parasitic turn-on at the CG edges. Fig. 14 clarifies that sufficient CG-to-channel distance results in a strong enhancement of the average program slope, experimentally verifying that the fringing field effects are minimized. Tailored tuning of cell structures and cell stack configuration has been carried out to maximize the average program slope for reduced-size cells.

BLK dielectric design is another key element for achieving adequate memory window with limited physical space. Incorporation of high-k BLK dielectrics, the first implementation in 3D FG cells, provides a potential approach for breaking through the trade-off relation between the program window and program saturation (Fig. 15). Compared to the SiN-based BLK, the high-k-based BLK enables higher coupling ratio to gain program window in conjunction with decreased electron leakage from the FG, thus relieving the saturation issue. The resulting experimental program/erase characteristics in Fig. 16 reveal that the high-k-based BLK

places the semicircular FG cell at a significant advantage over the circular CT cell. In the optimized semicircular FG cells, the average program slope is 0.96 V/V, reaching the ideal value of 1 V/V, and the program/erase window is substantially larger as compared to the circular CT cells.

The isolated FG confines charges into the storage layer, thus preventing charge spreading toward adjacent cells. The critical improvement item for the FG cells, on the one hand, is cycling endurance [7], where generation of traps and interfacial damages must be attenuated. As demonstrated in Fig. 17, careful tailoring of TNL film quality and interface formation processes sufficiently improves endurance and post-cycling data retention up to 10k cycling stress.

Fig. 18 (a) compares simulated QLC V_t distributions after programming between the semicircular FG cells and the circular CT cells utilizing the same poly-Si channel properties. Simulation parameters were thoroughly calibrated against experimental cell characteristics. The semicircular FG cells, having superior program slope and program/erase window, are expected to attain comparably tight V_t distributions at small cell size. Integration of low-trap channel into the semicircular FG cells, further decreasing fluctuation variability including random telegraph noise, is capable of more than four bits/cell, e.g., Penta-Level Cell (PLC) as projected in Fig. 18 (b).

V. SUMMARY

Novel 3D flash memories with the semicircular split-gate cells have been constructed, and comprehensive analyses of cell design requirements are conducted. In the split-gate cell design, the parasitic fringing field effect has a profound impact on the program slope and hence cell performance. The semicircular CT cells display intolerably low program slope caused by the residual leakage paths at the CG edges. It is experimentally demonstrated that the properly designed semicircular FG cells with the high-k-based BLK exhibit significant gains in the program slope and program/erase window over the larger-sized circular CT cells. These results confirm that the semicircular FG cell is a viable candidate for advancing the quest to boost bit density.

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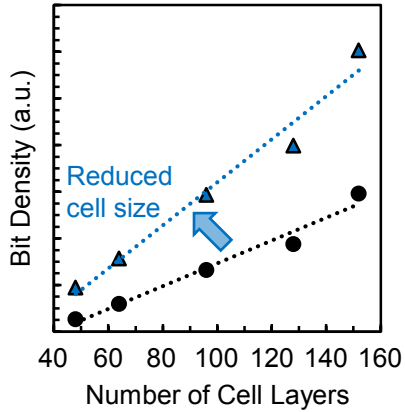


Fig. 1. Bit density as a function of the number of cell layers.

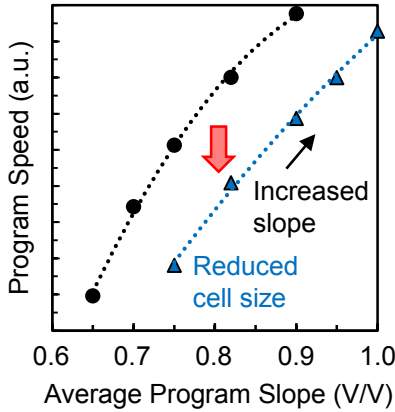


Fig. 2. Program speed as a function of average program slope.

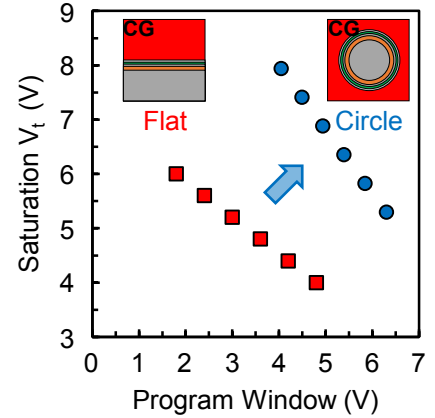


Fig. 3. Simulated results of saturation V_t versus program window.

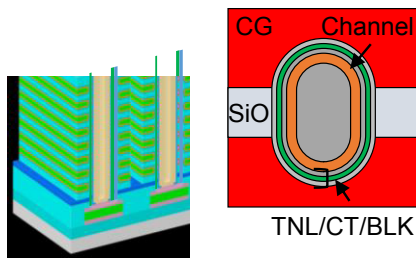


Fig. 4. Schematics of 3D cell architecture and plane view of the semicircular CT cells.

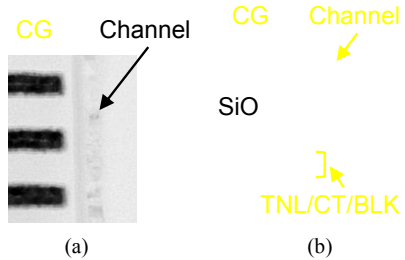


Fig. 6. Fabricated semicircular CT cells. (a) Cross-sectional view. (b) Plane view.

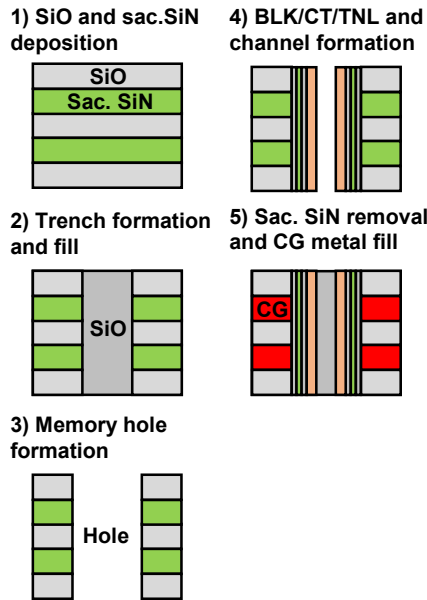


Fig. 5. Key process steps to fabricate the semicircular CT cells.

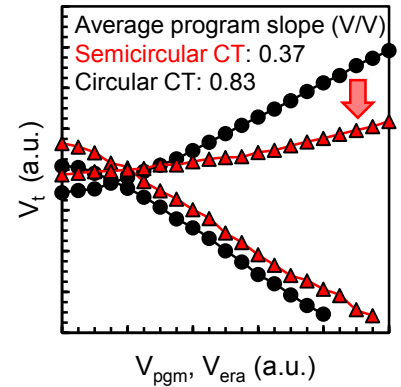


Fig. 7. Experimental program/erase characteristics comparing the semicircular CT cells with the circular CT cells.

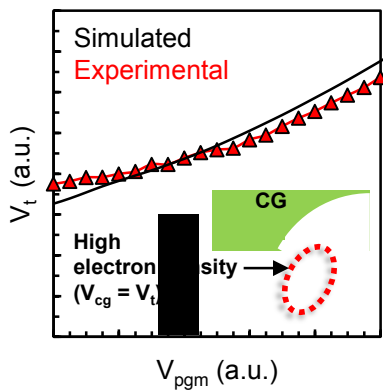


Fig. 8. Calibrated simulation results of the semicircular CT cells showing the parasitic leakage path induced by the fringing field.

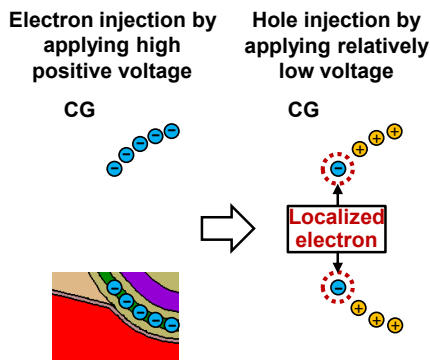


Fig. 9. Initial charge injection technique for introducing localized electrons at the CG edge regions.

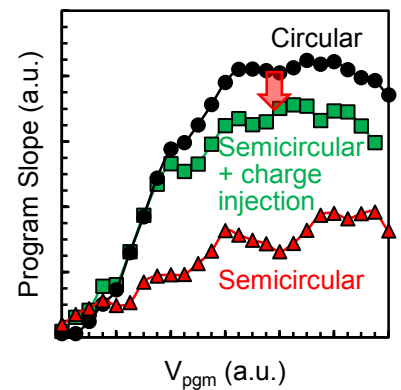


Fig. 10. Experimental program slope data comparing the semicircular CT cells with the circular CT cells.

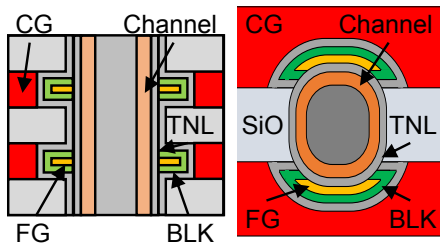


Fig. 11. Schematics of cross-section and plane view of the semicircular FG cells.

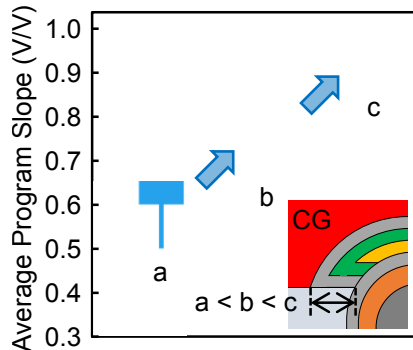
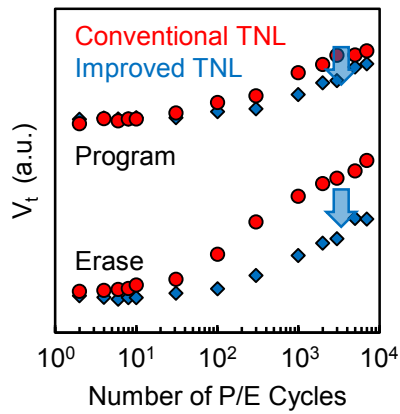
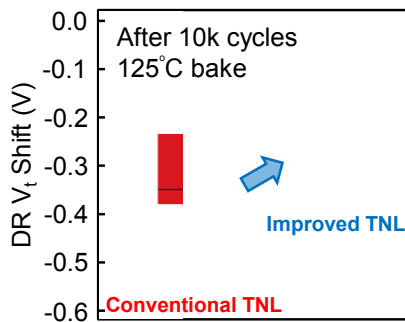


Fig. 14. Experimentally obtained average program slope for different CG-to-channel distances.



(a)



(b)

Fig. 17. Reliability for 10k P/E cycling stress. (a) Endurance. (b) Data retention.

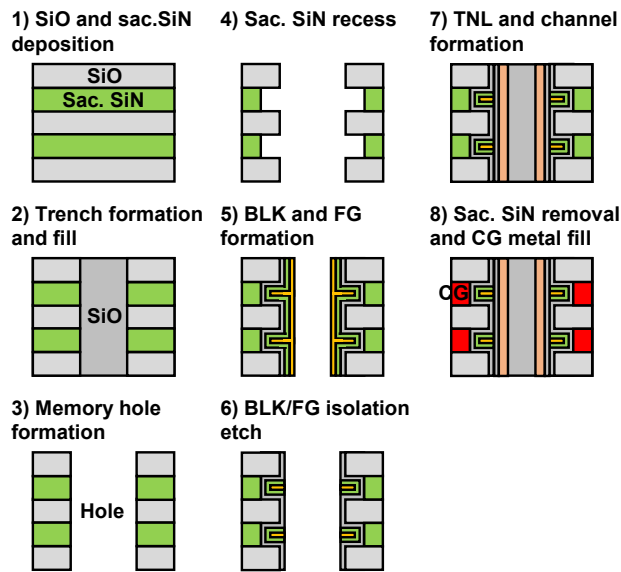


Fig. 12. Key process steps to fabricate the semicircular FG cells.

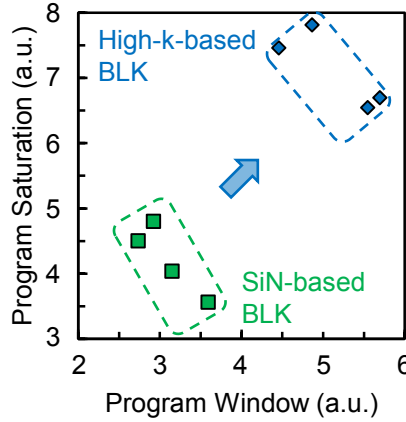


Fig. 15. Experimental characteristics of program saturation versus program window for different BLK dielectrics.

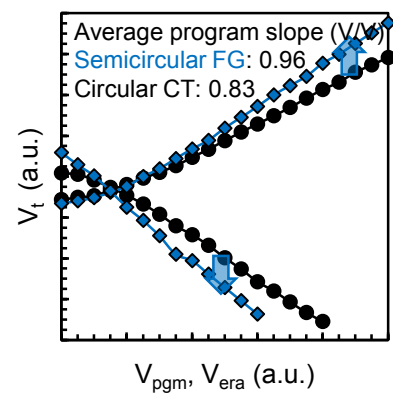
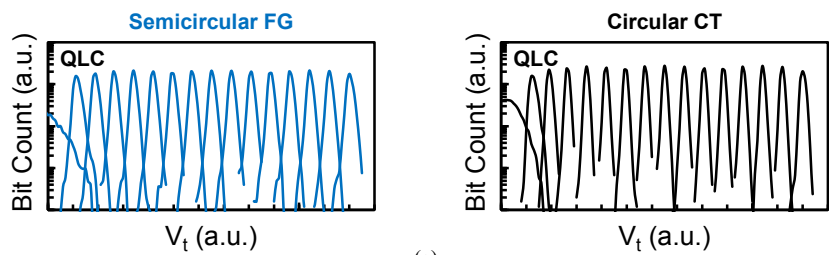
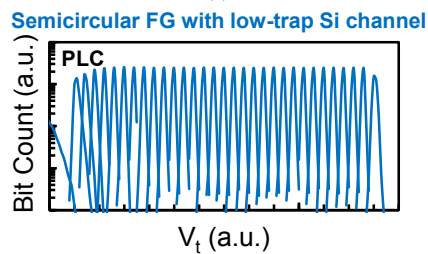


Fig. 16. Experimental program/erase characteristics comparing the semicircular FG cells with the circular CT cells.



(a)



(b)

Fig. 18. Simulated V_t distributions after programming using calibrated parameters. (a) QLC. (b) PLC.

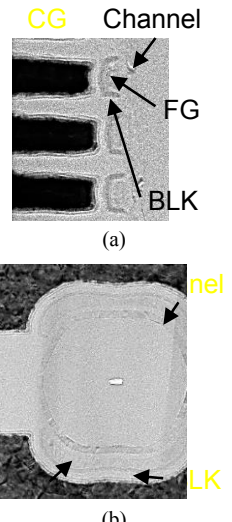


Fig. 13. Fabricated semicircular FG cells. (a) Cross-sectional view. (b) Plane view.