A 512Gb 3-bit/Cell 7th-Generation 3D NAND Flash Memory with 184MB/s Write Throughput and 2.0Gb/s Interface

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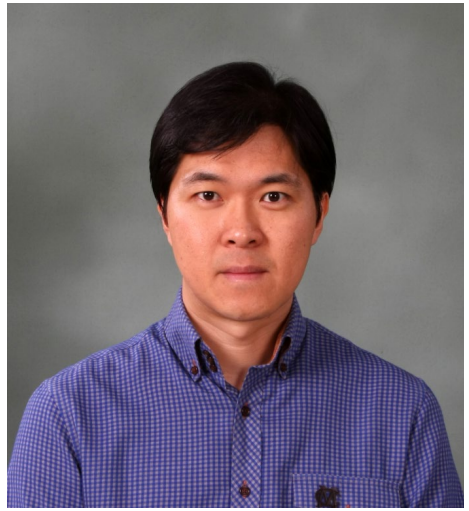
Samsung Electronics, South Korea

Self Introduction



Education Background

- B.S degree in Computer Science Engineering from Pusan National University, Pusan, South Korea, in 1998

Work Experience

- Have been with Samsung Electronics since 1998
- Designed Planar NOR/NAND Flash 1998-2012
- Designed VNAND [2^{nd} / 4^{th} / 7^{th} Gen.] since 2013 as Project Leader

Research Interest

- Memory Architecture / Circuit Design Cell Characteristic / Fault Analysis
- Business Strategy / Applications of Memory

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Technologies for 7th Generation 3D-NAND

Performance

- Conventional BL Forcing
- 2-step BL Forcing w/Dynamic latch
- 2-step BL/WL Forcing

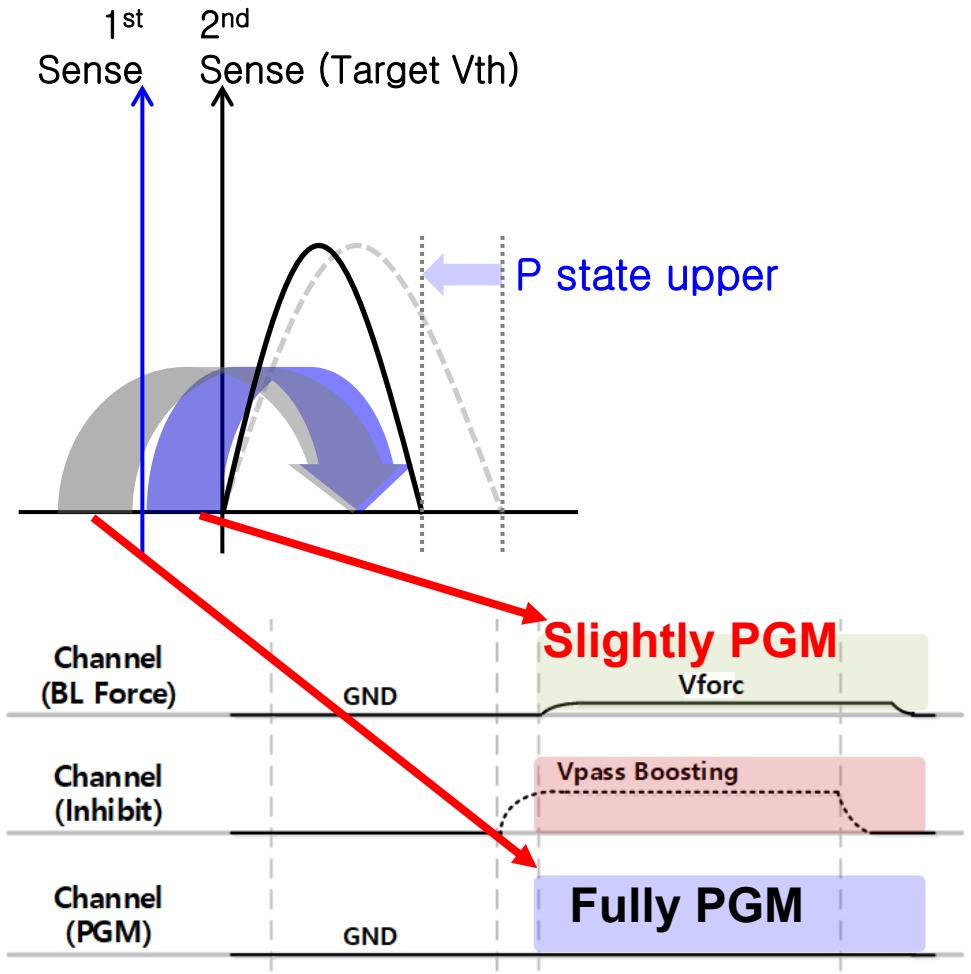
Power Consumption for COP Architecture

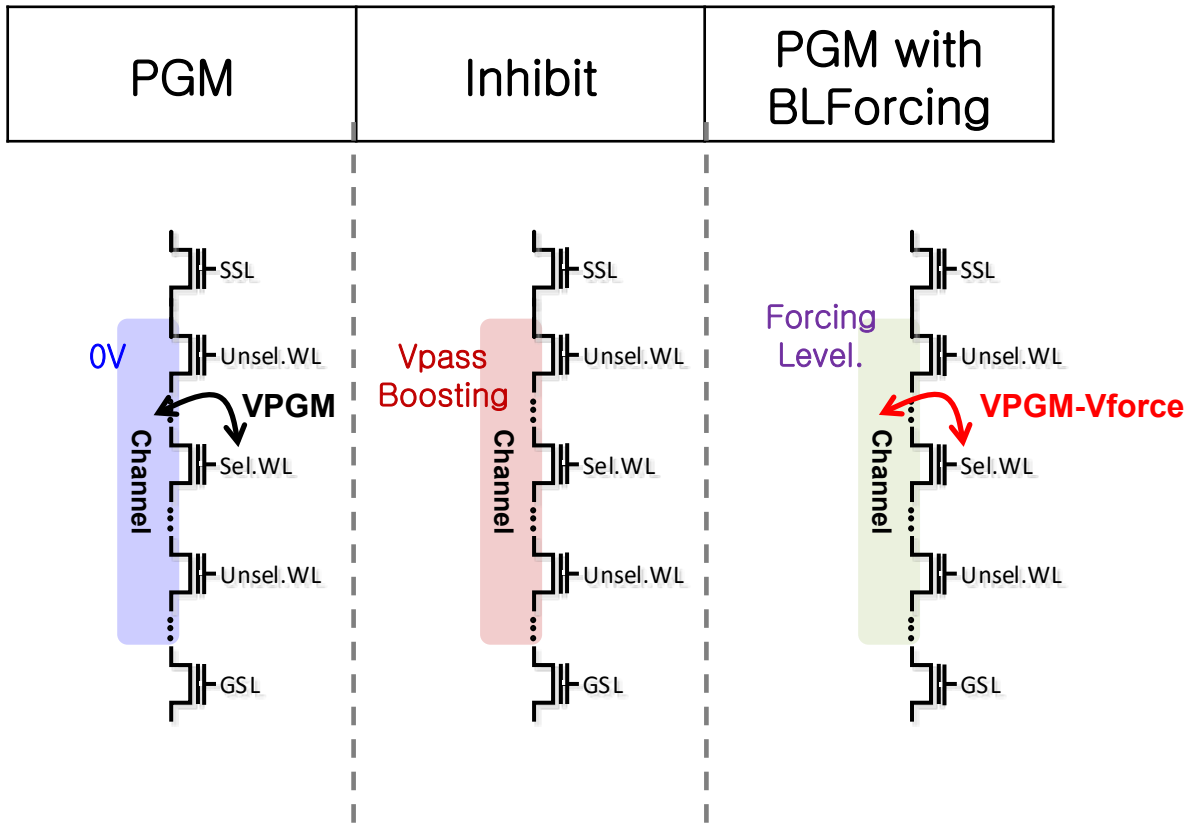
- MIM Cap for COP
- Optimization of Pumping Capacitors

2.0Gbps IO Support

- Dual Interface of Termination type

Conventional BL Forcing

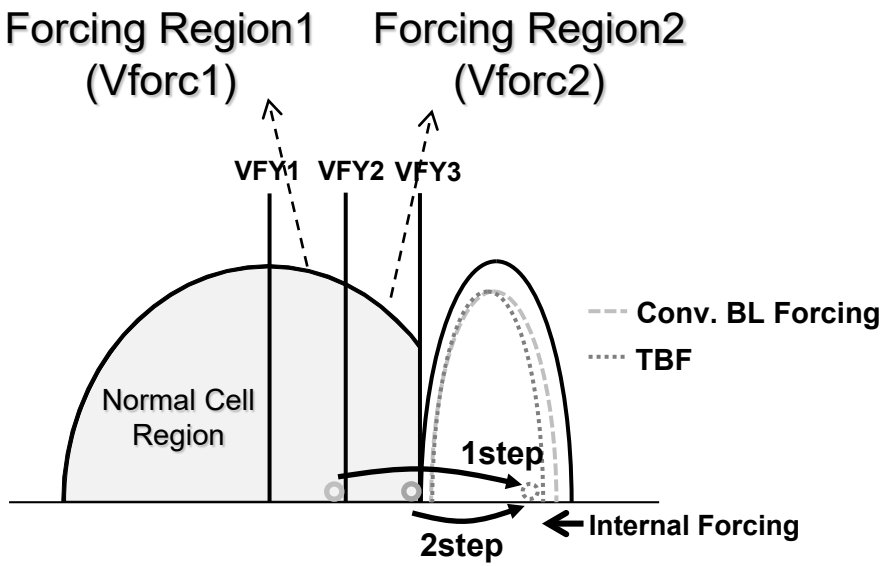




With BL forcing, the programming electric field between SEL WL and Channel is reduced.

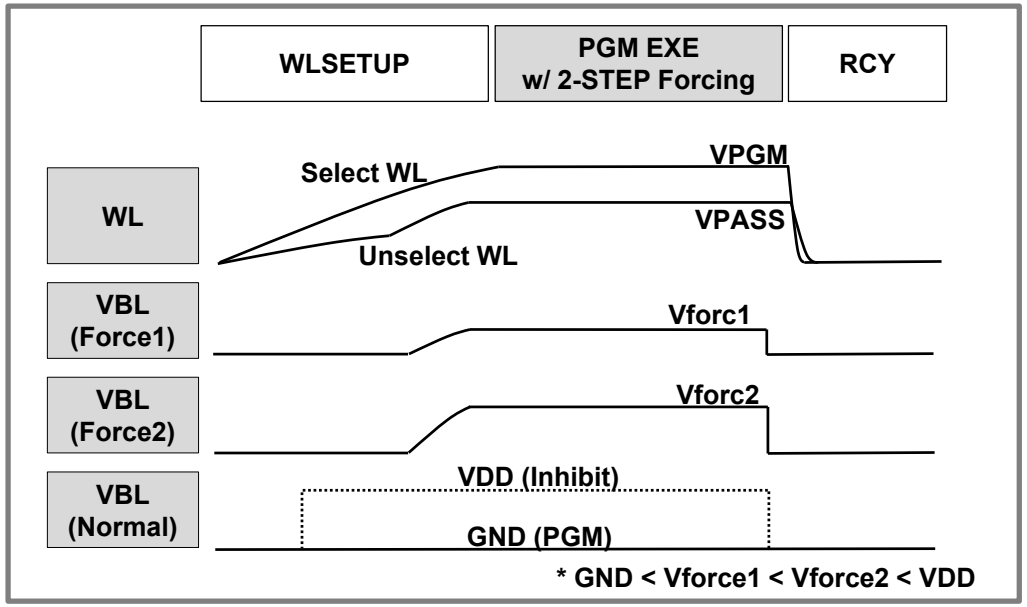
2-step BL forcing w/Dynamic latch

***Two-step BL Forcing**

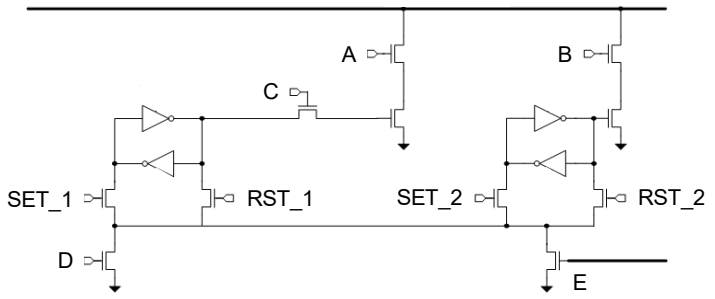


Concept of *TBF

Forcing Step1 & 2=> Upper Control



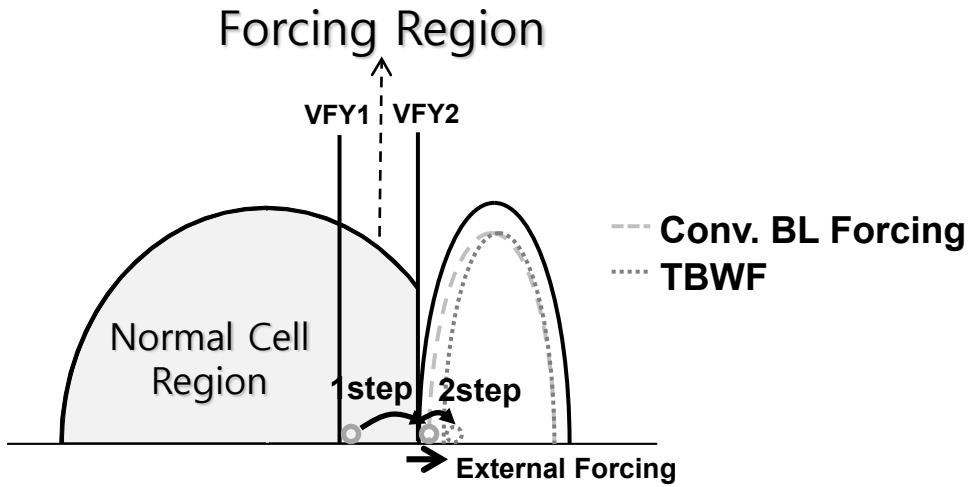
Timing Diagram of TBF



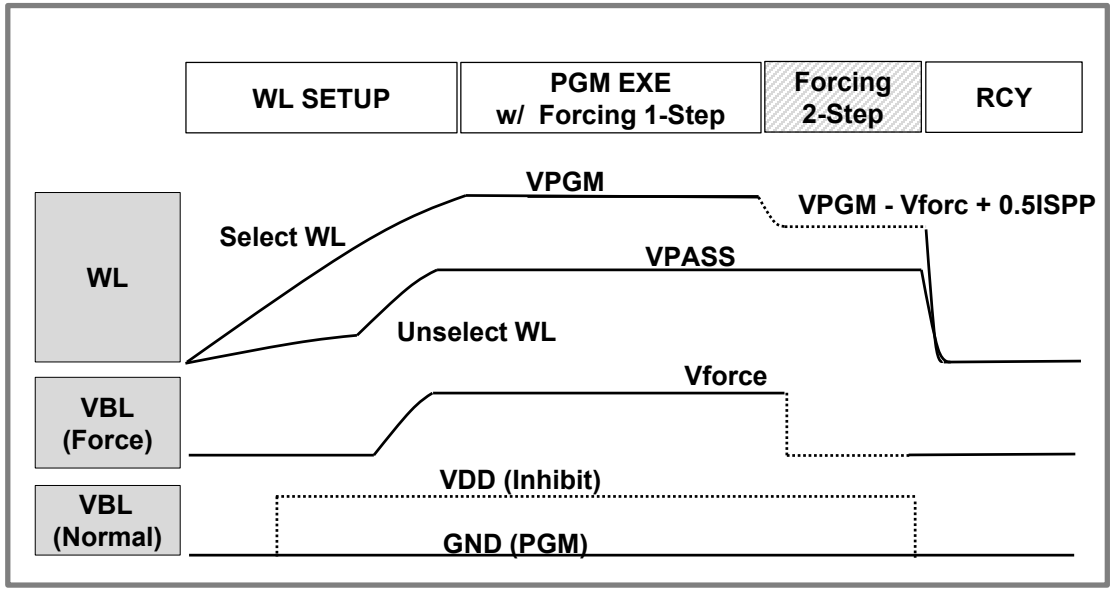
Dynamic Latch with TBF

2-step BL/WL forcing

***Two-step BL/WL Forcing**



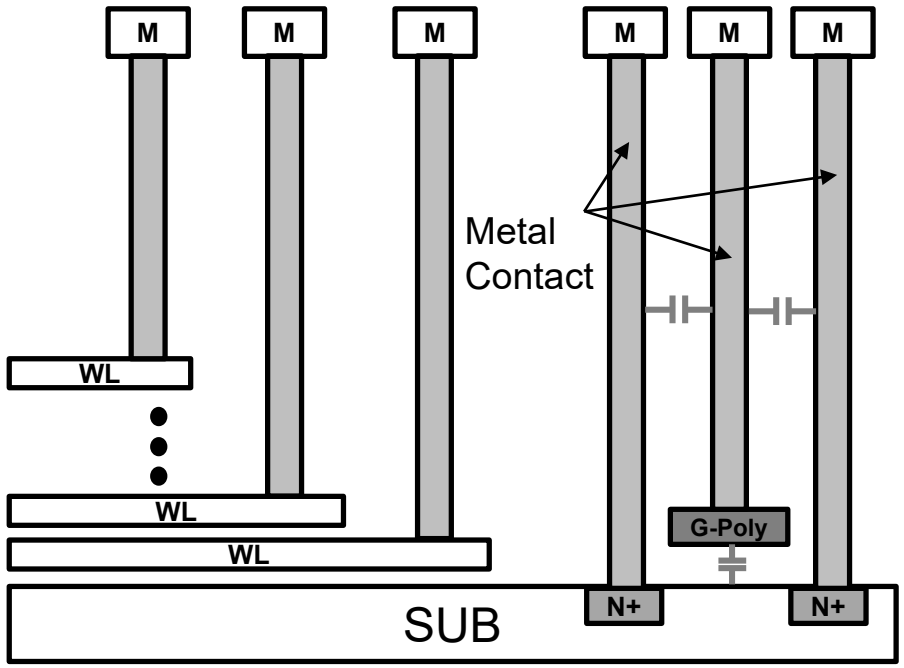
Concept of *TBWF



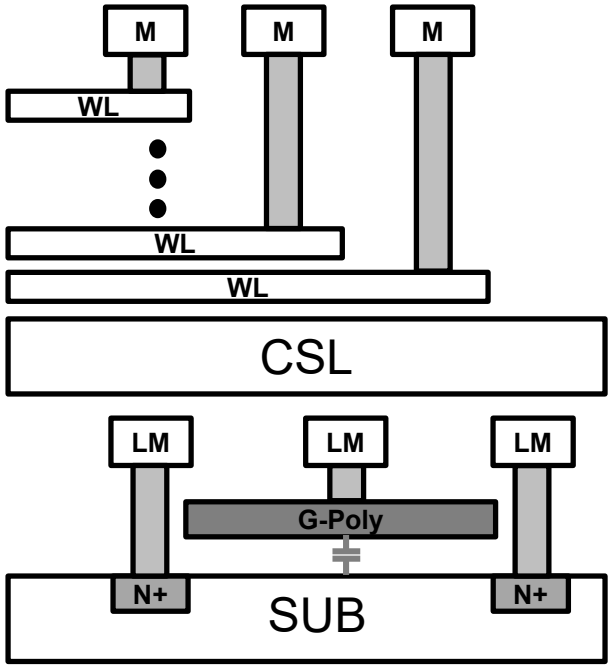
Timing Diagram of TBWF

Forcing Step1 => Upper Control
Forcing Step2 => Under Control

Comparison of Pumping Cap. Structures



Conventional Architecture

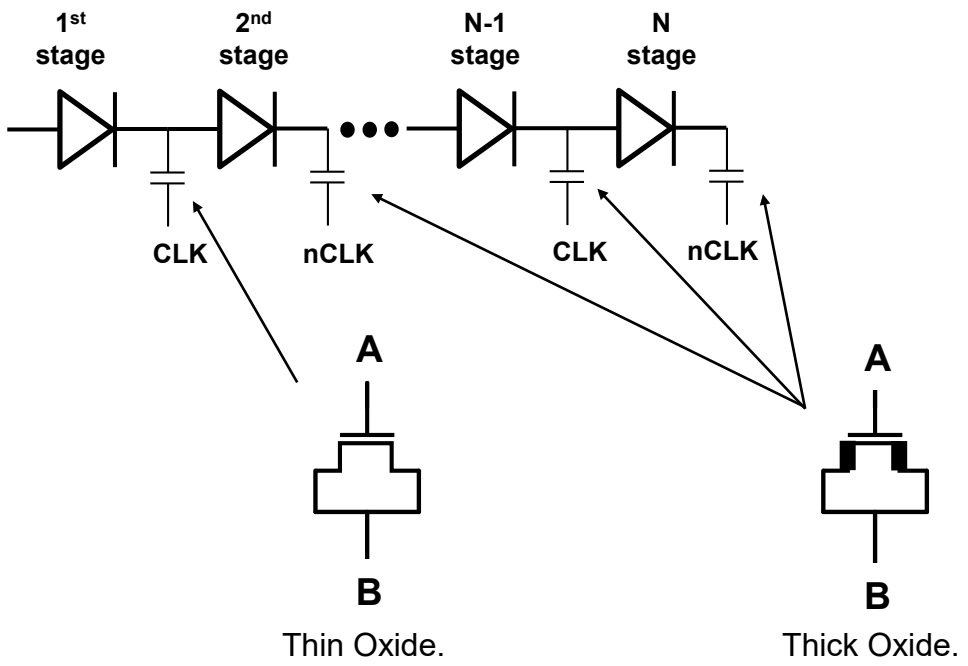


Cell Over Peri Architecture

Comparison of pumping capacitors of 3D NAND

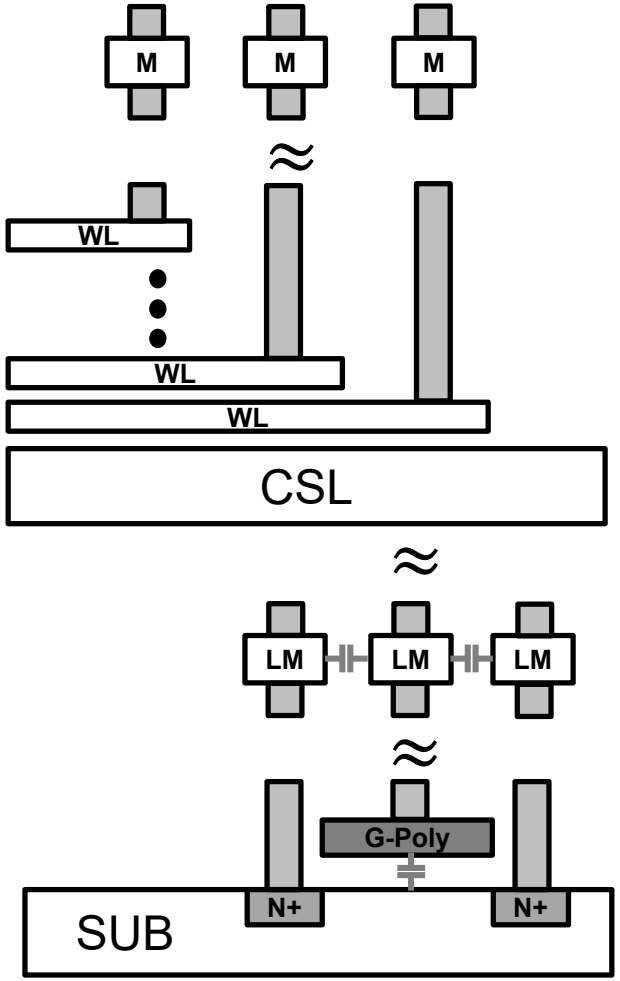
Pumping capacitors of metal contact is not available in Cell Over Peri Architecture.
So, power and area efficiency of charge pumps is degraded

1st Stage LVN Cap. & MIM Cap for COP



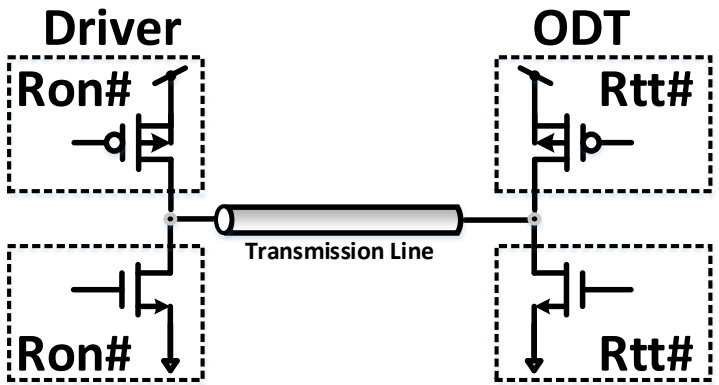
Optimization of pumping capacitors by series stage

1st Stage LVN Cap. & MIM caps for COP achieve 24% power reduction and 27% area reduction of charge pumps



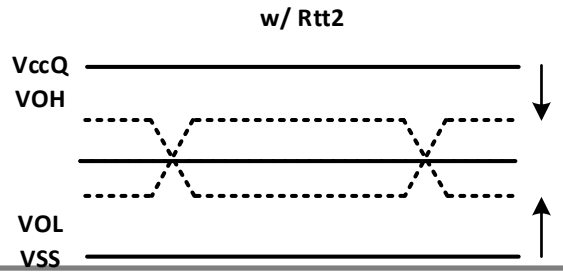
MIM caps for COP

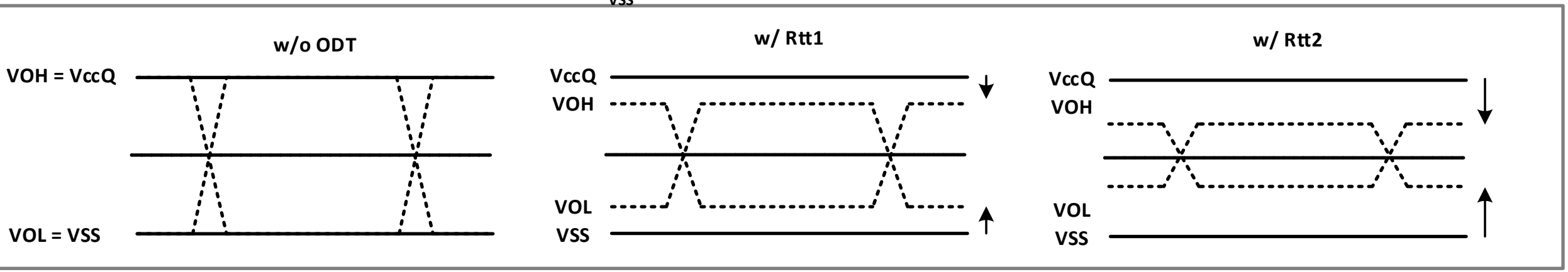
Toggle 4.0 Interface



Driver & ODT

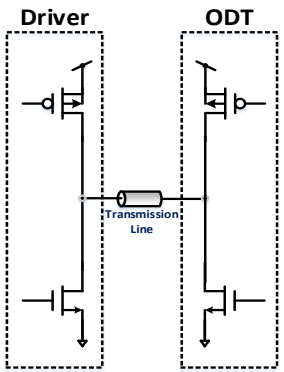
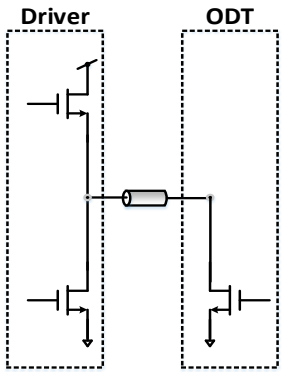
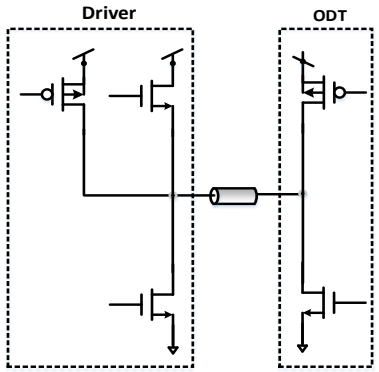
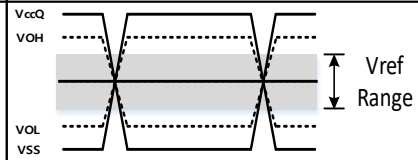
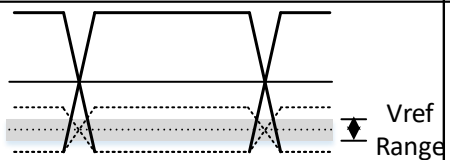
For high speed SI, using strong ODT is required.
But it increases channel power consumption.





CTT Interface Signaling

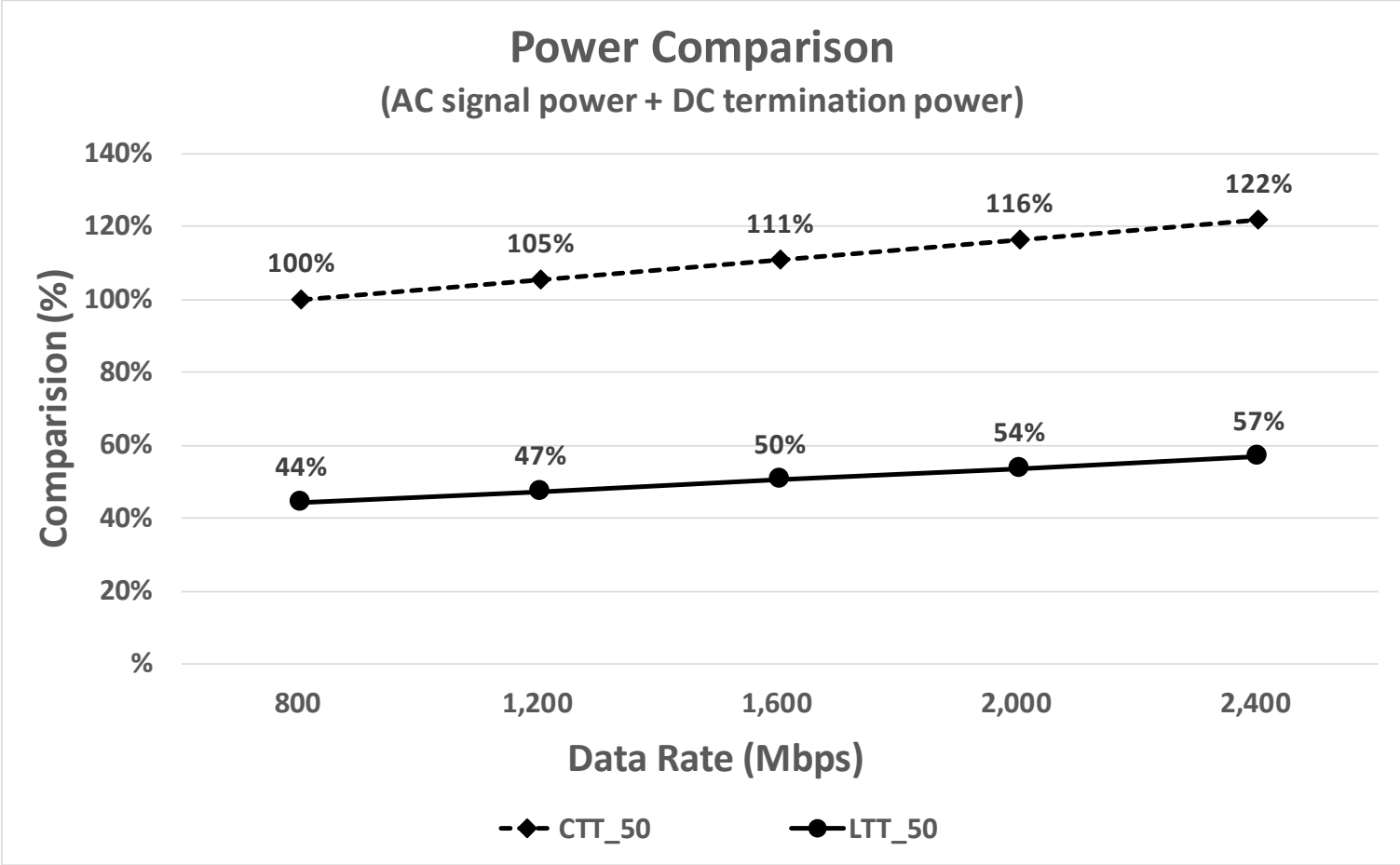
Dual Interface

Interface Type	(A) CTT	(B) LTT	(C) V-NAND 7th Gen (Dual interface)	
Circuit Topology				
Signaling			= CTT @ CTT mode = LVSTL @ LTT mode	
Tr. type			CTT mode	LTT mode
Pull Up	PMOS	NMOS	PMOS	NMOS
Pull Down	NMOS	NMOS	NMOS	NMOS

Comparison of Interface type

Dual Interface : In heavy load systems, select CTT interface mode and in lighter-load systems select LTT interface mode.

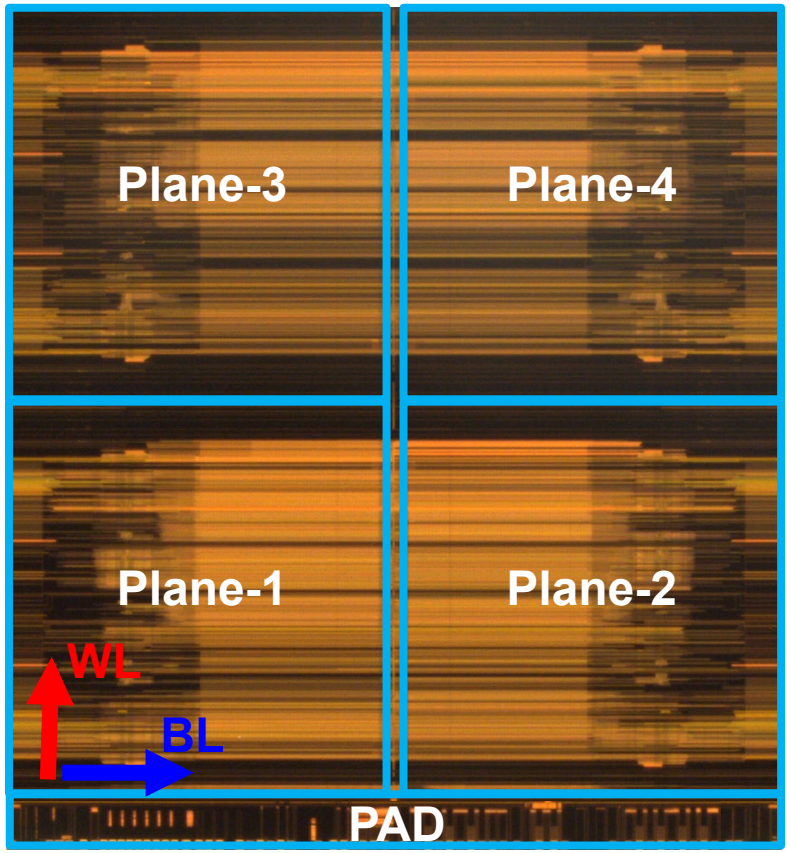
Power comparison



Termination type Power comparison

At 2Gbps I/O speed, 62% channel power reduction in LTT interface than in CTT interface.

Conclusion - 7th Generation 512Gb 3D NAND



Die photograph

	ISSCC 2019[1]	This Work
Bits per cell	3	3
Density	512Gb	512Gb
Page Size	16KB/Page	16KB/Page
Bit Density	5Gb/mm^2	8.5Gb/mm^2
I/O Bandwidth	Max. 1.2Gb/s	Max. 2.0Gb/s
tBERS	3.5ms (Typ.)	3.5ms (Typ.)
tR	45us	40us
Program Throughput	82MB/s	184MB/s
Vcc	2.35V to 3.6V	2.35V to 3.6V
Vccq	1.2V	1.2V

Feature Summary