Development of a 3D stacked package solution for NAND 64DP package

Kerry Yang, Mark Barney, Liana Foster, Elyn Xu, Mark Hall

***Abstract* — The need for high stacked NAND package is driven by solid state drives. Customers generally want more NAND density per package placement. Stacking chips into the vertical or third dimension (3-D) has evolved into the stacking of packages to meet the marketing needs. The advantages of stacking packages rather than chips is that the packages inside can be fully tested and ensure known good part prior to stacking. The development and evaluation work of 64DP packages was accomplished through close co-working of multi-teams especially assembly, product engineering and quality engineering. This paper describes the challenges in the process development, reliability testing; and failure modes observed during the qualification.**

***Index Terms* — Package-in-package (PiP); Three-dimensional packaging (3-D); Intermediate testable modules (ITM);**

I. Introduction

Solid-State-Drives (SSD) don't have mechanical components [1]. This distinguishes them from traditional electromechanical magnetic disk such as hard disk drives (HDD). Compared with HDD, SSDs are typically more resistant to physical shock, and have faster access time and less latency. SSD prices are higher per unit of storage than consumer-grade HDD [2]. Most SSDs use NAND-based flash memory. NAND flash has become a very important component of SSD. The falling prices and increasing densities will be critical for SSD future. These requirements drive the high stacked NAND development.

Current NAND packages have achieved 8 die package (DP)/16 die package (DP) successfully. Higher stack packages have lower yield due to killer defects from stacking and are caught during backend electrical testing. The biggest advantages of stacking packages rather than device chips is that the packages can be fully tested good prior to stacking, which will improve the backend yield significantly.

This is the maximum yield loss calculation. The actual yield will be more than these calculations. Fig. 1 shows that the stacked package backend test yield reduces significantly with the increase in stack height. This is a big challenge for process improvement to achieve higher yield for high stack packages.

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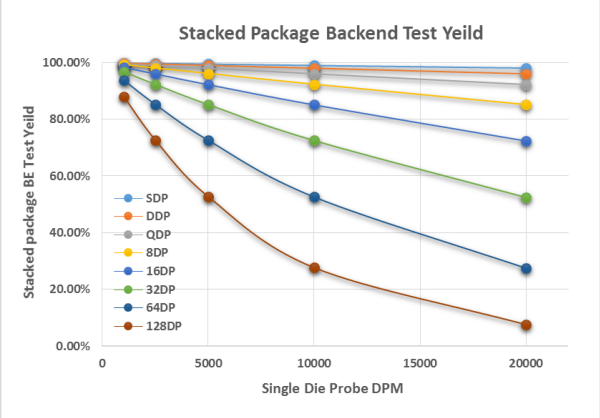

Fig. 1. Backend test yield vs. assumed probe DPM

By using known good 16DP packages to build 64DP (package in package construction), yield could be improved from 72.6% to 92.3% assuming probe DPM is 5000 and no yield loss from assembly. Package-in-package (PiP) technology was introduced to stack different function packages together using wire bonding process to support cellular handsets and mobile products [3][4][5].

It was reported that PiP variations with two-die stacked are already in mass production [4]. There was no 64DP package reported yet. This paper is to introduce the 64DP technology development with stacking 4 Internal Testable Modules (ITM) of 16DP package and associated assembly process challenges and reliability performance (Fig. 2)

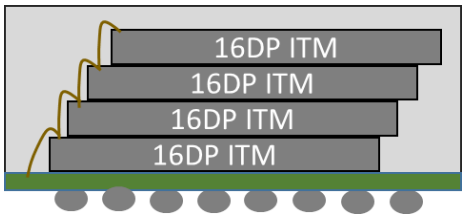

Fig. 2. 64DP Package-in-package construction

II. Assembly Process

Enterprise SSD generally demands high NAND capacity with constraints on XY space while flexibility in Z direction. The packaging solution developed in this work is to stack four 16DP packages in Z-direction into one package. The 16DP ITM is 14x18x1.13mm in size and is a very thin Land Grid Array (LGA) type of Fine Pitch Ball Grid Array (FBGA) package. It has an array of landing pads in order to be tested using commercially available test sockets. It also has a row of bond

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fingers at the edge of the package that allow wire-bonding interconnects to the PiP package substrate.

A. Package Architecture

The stacked ITM package is a known good part. It has been fully qualified. The stacked package has 15x21x5.7mm dimensions. The height of 5.7mm is a big challenge to the wire bond and the encapsulation processes due to 5.15mm mold cap. The substrate is 4 layers laminated with electrolytic Ni/Au finish on the wire bonding fingers. Table 1 shows the package in package configuration.

Table 1. 64DP package in package configuration

Description	**272 TFBGA**
Package Body W x L x H	15.0 x 21.0 x 5.7 (mm)
Mold Cap Thickness	5.15mm
Substrate Thickness	0.21mm 4Layer
ITM stack	Shingle
Surface Finish	Electrolytic Ni/Au
BF pitch/width (back side)	85/60 um

B. Assembly Process Challenge

The package process is similar to chip die attach package process. This is a standard 16DP with reverse shingle-on-shingle structure completed packages without solder balls. The known good 16DP ITM package is flipped upside down and attached with epoxy. Repeat ITM attach process and pre-cure after stack each layers. Pre-WB (wire bond) Plasma clean is performed before the wire bonding process to ensure the clean wire bonding Cu lead finger. Shingle cascade bond method is adopted to bond the re-route bond fingers on what is normally ball-side of 16DP from one packages to another. The assembly process flow is shown in (Fig. 3).

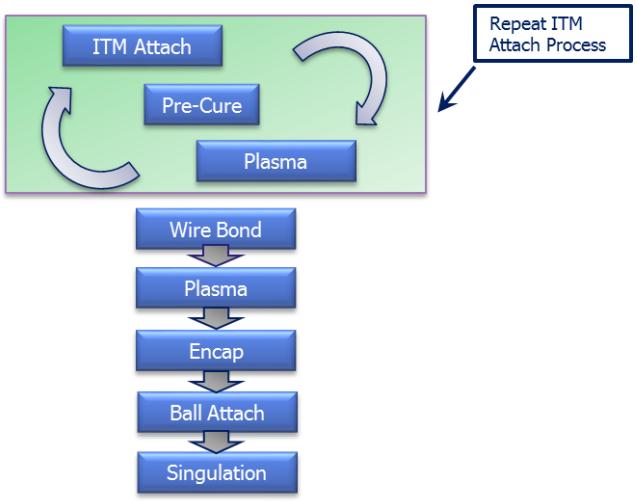

Fig. 3. Assembly process flow

The most challenging part during assembly is the wire bond process due to 5mm super high stack. To minimize cone angle and maximize bottleneck height and achieve minimum wire-to-wire pitch and die edge to bonding finger edge, a low risk and low cost solution was adopted as cascade shingle bonding method, as shown in Figure 4 wire bond profile. This eliminated the extremely long wires that can short together if not straight. The wire consumption is around 60% less for this method.

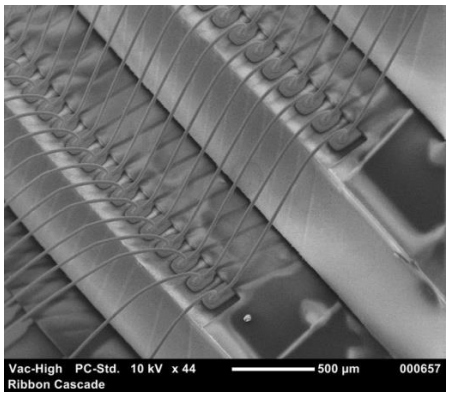

Fig. 4. Wire bond profile

Pull min value from wire bond integrity pull test is 9.5gmf and average pull force is 11gmf (Fig. 5). Both values are within JEDEC specification and there is no abnormal fail mode observed [6].

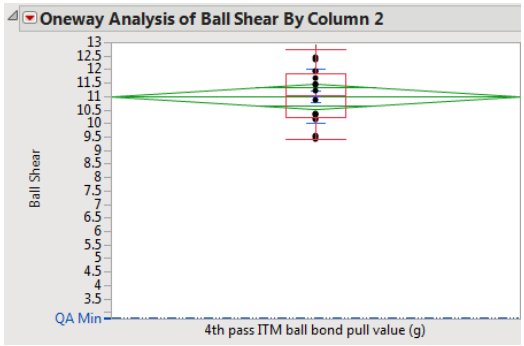

Fig. 5. Wire bond pull distribution

The development team tried different kinds of encapsulation method to mold the thick package, which is the other most challenging part. Liquid mold method and top gate mode process have been adopted to build the engineering lots. The cross-section view of an actual PiP is shown in (Fig. 6).

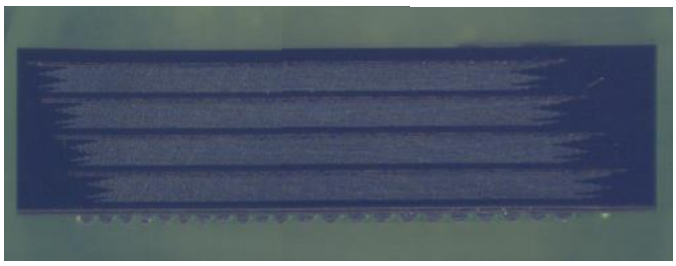

Fig. 6. Cross section view of an actual PiP package

There were four 16DP packages stacked inside with die

attach epoxy to attach each ITM package together. All 16DP ITMs have gone through backend electrical test. During evaluation, die attach void or delamination was found with no clear evidence pointing to the contamination issue. The package cleaning process to ensure all contamination involved during backend test are removed, will be evaluated when this projects move to next qualification stage followed by release for mass production.

III. Package Qualification Reliability Tests

A. Live-die Pathfinding with Liquid Mold Method

Moisture Sensitivity Test (MST) is a characterization test used to assess the classification level of moisture sensitive devices [7]. Level 3 test is generally accepted as a minimum requirement in the industry to ensure sufficient floor life for most surface mount processes. Table 2 lists MST level test conditions.

Table 2. MST level test conditions

Level	Floor Life	Soak Requirement	
		Standard	Accelerated Equivalent
MST L2	One year <=30 ºC /60%RH	168hrs 85ºC/60%RH	N/A
MST L3	168hrs <=30ºC/60%RH	192hrs 30ºC/60%RH	40hrs 60ºC/60%RH

During PiP path finding, the liquid mold encapsulation method was used in the first live-die build. Two gross delamination fails were observed during MST L2 test as shown in (Fig. 7) by Confocal Scanning Acoustic Microscope (CSAM).

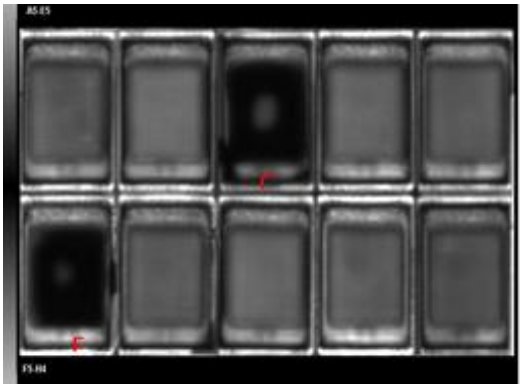

Fig. 7. CSAM image with delamination in 2 parts

The cross-section of the part "C" confirmed that the package crack starts from the bottom of ITM edge as shown in Figure 8. It was suspected that the mold compound used in liquid mold couldn't survive the internal stress. The crack was not seen in the next build when moved to different molding process with different molding material.

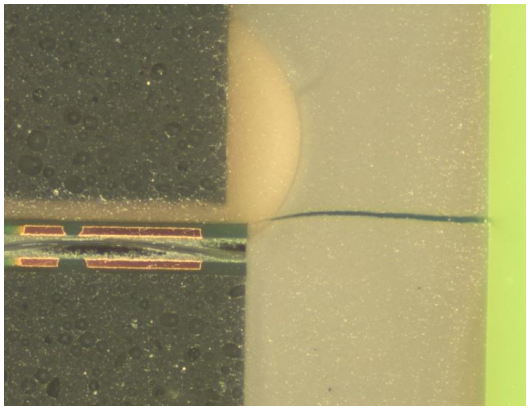

Fig. 8. X-section image of crack in the package

If delamination of the fail part is less than 2/3 from die edge to package edge, it could be accepted if the part passed the further evaluation based on JEDEC guidelines [7]. This kind of fail is named soft failure. There were 3 soft delamination fails during MST L3. While in the follow up Temp Cycling JEDEC condition B (-55ºC to -125 ºC, T-C/B), all of these 3 soft fails failed electrical test with substrate/solder mask massive delamination and were downgraded (Fig. 9). It was suspected that the 2-layer substrate couldn't survive the high stress induced by the high stack. In the next evaluation, a 4-layer substrate didn't produce the same issue.

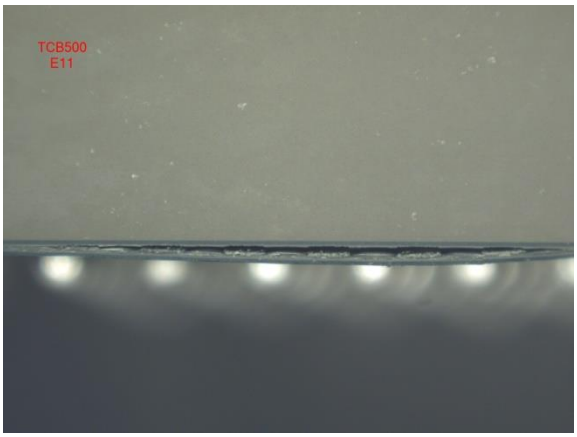

Fig. 9. Delamination between substrate and solder mask

The data is summarized in Table 3. This data was collected from first PiP stack build from 4 ITM packages. Package failed MST L2/L3 and T-C/B tests but it validated the feasibility of stacking the ITMs From these fails, it was identified that the liquid mold method was not reliable for PiP package.

Table 3. First PiP live build test results

Test Items	Test Result (failed/total units)	Fail Modes	Conclusion
MST L2	2/34	Gross delamination	Fail
MST L3	0/34	Soft delamination fail	Fail
T-C/B 500cycles	4/34	Substrate/solder mask crack	Fail

B. Live-die Pathfinding with Top Gate Mode Method

Top gate encapsulation method was adopted to continue pathfinding for the best solution for PiP assembly technology. Four lots were built for reliability testing. The first lot was sampled MST L2 without any fail (0/30u). The other three lots were subjected to soak L3 Accelerated (ACC) preconditioning with extended Temp Cycling JEDEC B condition (-55ºC to -125 ºC, T-C/B). During L3ACC sampling, two lots didn't have any delamination. But one lot (lot#3) had delamination attributed to incoming material issue as shown in Table 4. All parts from this lot showed time zero delamination before starting any stress test. After soak L3ACC preconditioning test, five units delaminated massively, suspected to be caused by moisture trapped in the delaminated surfaces (Fig. 10).

Table 4. CSAM results of 1K T-C/B with L3ACC Pre-con

Assembly lot	Pre-L3acc Pre-con CSAM	Post-L3acc Pre-con CSAM	500x T-C/B CSAM	1000x TCB CSAM
Lot #1	0/22	0/22	0/22	0/22
Lot #2	0/27	0/27	0/27	0/27
Lot #3	31/31	31/31	31/31	30/30

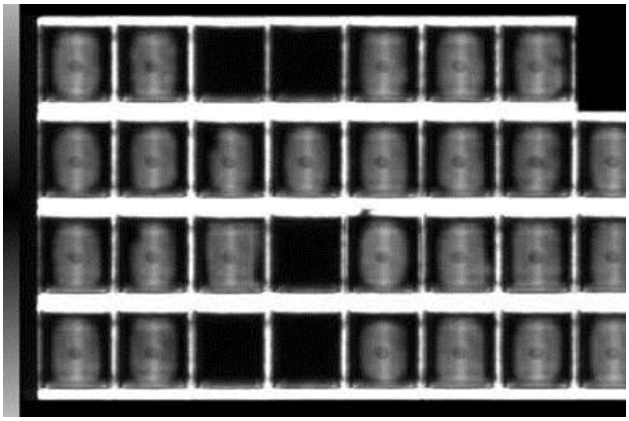

Fig. 10. CSAM images for 3rdlot: delamination in all parts

Physical cross-section image revealed that delamination happened between the ITM mold compounds and the package attach epoxy material (Fig. 11). It pointed to the possible process deviation during ITM attaching process.

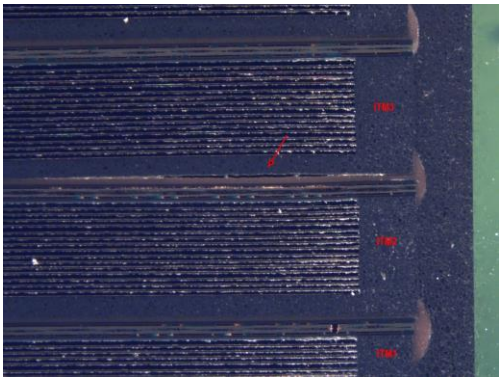

Fig. 11. X-section images of the delaminated part

There was no electrical fail associated with any delamination observed from pretest to 1000 T-C/B cycles as shown in Table 5. The 3rd lot didn't have any package related fallout even with all parts showing delamination. There was one device related fail and was identified not to be related to any assembly process or package.

Based on the passing MST L2 and T-C/B results for first two lots and 100% fail at time zero for the 3rd lot, a process deviation or miss-processing of the 3rd lot is suspected. The package process concept is considered capable with further continuous improvement plan required for full understanding. Technology development is suggested to move forward to next developing phase. And at next phase, the delamination issue will be re-evaluated along with other reliability evaluations to assess the process.

Table 5. Test result of 1K T-C/B with L3ACC Pre-con

Assembly lot	Quantity	Pretest	500x TCB Electrical Test	1000x TCB Electrical Test
Lot #1	22	0/22	0/22	0/22
Lot #2	27	0/27	0/27	0/27
Lot #3	31	0/31	1*/30	0/30

*Device related fail, it was identified not related to assembly processing

IV. Further Developments

The packaging technology described in this paper is expected to be applicable to products from different technology nodes by replacing the internal testable modulus. Further development work is needed to develop stable assembly process to make it more suitable for mass production. Further work also need to consider how to shrink the package size, reduce the total package height, and further optimize of the internal ITM as well.

V. Conclusion

A new 3D package PiP technology has been described. Several challenges were encountered notably: ITM attach process, wire bonding process and the encapsulation process. Some of these challenges have been overcome but still require further optimization. The future evolution of the PiP technology will need to pass all required reliability qualifications to assess the process capability and stability.

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