Technical Note

ONFI 4.0 Design Guide

Introduction

The ONFI 4.0 specification enables high data rates of 667 MT/s and 800 MT/s. These high data rates, along with lower input/output capacitance, C_{IO}, that enables more die stacking, introduces new challenges to the optimum design of NAND memory systems and solid-state drives (SSDs). This technical note provides some guidelines for the design of the NAND memory system or SSD. The end users are expected to perform system simulations and hardware characterization through laboratory measurements to verify their system designs.

The following technical notes are available for reference on micron.com:

- TN-00-20: Understanding the Value of Signal Integrity Testing
- TN-29-77: Chip Enable Pin Reduction in NAND Flash Devices
- TN-41-13: DDR3 Point-to-Point Design Support
- TN-52-02: LPDDR2/LPDDR3 Point-to-Point System Design
- TN-29-58: ONFI NV-DDR2 Design Guide

What Is New in ONFI 4.0?

ONFI 4.0 introduces the NV-DDR3 data interface and continues to support all previous data interfaces, namely SDR, NV-DDR, and NV-DDR2.

ONFI Data Rates

Table 1 shows all available timing modes for different data interfaces. ONFI 4.0 NV-DDR3 has the same timing modes as ONFI 3 NV-DDR2, but also introduces timing mode 9 and 10 which are 667 MT/s and 800 MT/s operations, respectively.

Table 1: ONFI Data Rates

Timing Mode	Data Rate				Unit
	SDR	NV-DDR	NV-DDR2	NV-DDR3	
0	10	40	67	67	MT/s
1	20	67	80	80	
2	29	100	133	133	
3	33	133	167	167	
4	40	167	200	200	
5	50	200	267	267	
6	–	–	333	333	
7	–	–	400	400	
8	–	–	533	533	
9	–	–	–	667	
10	–	–	–	800	

ONFI Feature Comparison

Table 2 summarizes some of the features comparison in different ONFI and data interface standards. From ONFI 2.3 to ONFI 3.2, new features were introduced include differential signaling for DQS and RE_n signals, warm-up cycles, and on-die termination (ODT). The maximum data rate was also increased to 533 MT/s.

Table 2: ONFI Data Interface Feature Comparison

Feature	ONFI 2	ONFI 3	ONFI 4	
	NV-DDR	NV-DDR2	NV-DDR2	NV-DDR3
DQS and RE_n	Single ended	Differential, optional	Differential, optional	Same as NV-DDR2
Warm-up cycles	No	Yes, optional	Yes, optional	Same as NV-DDR2
CA signal data rate	50 MT/s	Same as NV-DDR	Same as NV-DDR	Same as NV-DDR
Package electrical specification	Pin capacitance (package + die capacitance)	Similar to NV-DDR, values may differ	Z_{PKG} and T_d	Z_{PKG} and T_d
ZQ calibration	No	No	Yes, but not available for $R_{on} = 25\Omega$	Yes
Input/output capacitance C_{IO}	Specified with package, varies with number of LUNs	Same as ONFI 2	2.5pF MAX[1]	2.5pF MAX[1]
Maximum overshoot/undershoot voltage	1.0V	1.0V	1.0V	0.8V
ODT support	No	Yes	Yes	Yes
V_{CCQ} support	3.3V or 1.8V	1.8V	1.8V	1.2V
Maximum speed	200 MT/s	533 MT/s	533 MT/s	800 MT/s

Note: 1. Refer to each device data sheet for actual C_{IO}. Micron ONFI 4.0 compatible devices have significantly lower die capacitance when compared with ONFI 3.0 compatible devices.

For ONFI 4.0, major differences include:

- introduction of ZQ calibration
- lowering the V_{CCQ} voltage from 1.8V to 1.2V
- lowering maximum overshoot/undershoot voltage to 0.8V
- new parameters of characteristic impedance (Z_{PKG}) and package time delay (T_d) to specify package electrical characteristics

For ONFI 2.x and ONFI 3.x, the total package and die capacitance were specified. For ONFI 4.0, the package is specified in terms of characteristic impedance (Z_{PKG}) and package time delay (T_d). This means that the inductance of the package is taken into account. The new specification enables engineers to compute reflections due to impedance mismatch. It also enables user to predict skew and timing mismatches more precisely.

ONFI 4.0 NV-DDR3 drive strengths are 50Ω and 35Ω. ONFI 4.0 NV-DDR2 supports drive strengths of 50Ω, 35Ω, and 25Ω. However, ONFI 4.0 NV-DDR2 does not have ZQ calibration for 25Ω.

ZQ Calibration and ODT Setting

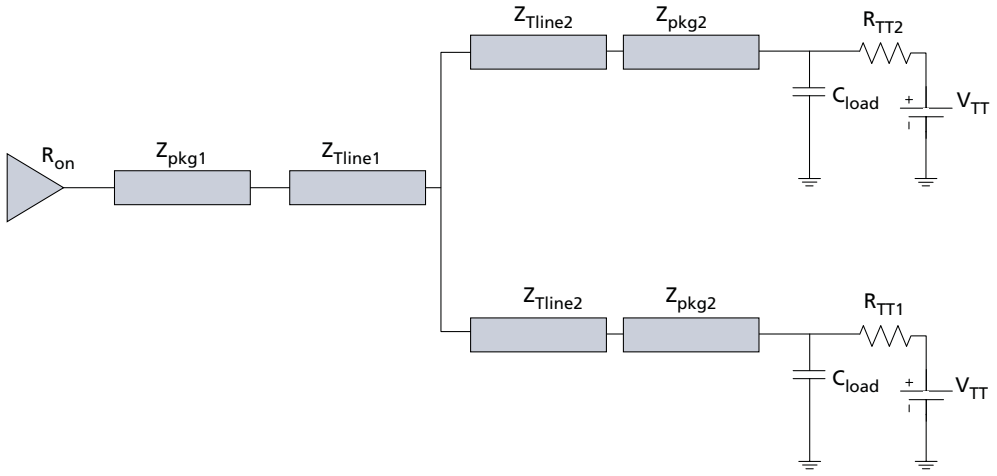
ONFI 4.0 introduces ZQ calibration. By connecting a 300Ω resistor (±1%) to the ZQ pin, the internal drive strengths and ODT values can be calibrated to this resistance. This means that the variances on the drive strengths and ODT values are reduced. The error is about 15% with ZQ calibration and 35% without ZQ calibration.

Due to R_{ZQ} value of 300Ω, ONFI 4.0 has ODT settings of 150Ω, 100Ω, 75Ω, and 50Ω.

Design Guidelines for Tree Topology

Many multi-package SSDs are routed using the tree topology, at least for the DQ bus. Figure 1 shows an SSD system with two NAND packages arranged in a tree topology in write mode.

Figure 1: SSD System with Two NAND Packages in Write Mode



The transmission line that leads to the package without the receiver essentially acts like a stub. Terminating the end of the stub would reduce reflections and improve the signal quality at the receiver. For a multi-die package, the termination can be placed on one or two of the dies (LUNs) on the same channel. The choice of die to be terminated likely does not affect the system performance. The value of the termination resistance (R_{TT1} and/or R_{TT2}) has to be determined from simulations and confirmed with measurements.

For data rates of 400 MT/s and 533 MT/s, Micron's internal guideline is to have ±5mm length tolerance on Z_{Tline1} among DQ traces on the same channel. This is to reduce skew among the traces. The length of 5mm translates to a 33.4ps delay on a stripline in a substrate with a dielectric constant of 4. This is less than 2% of the unit interval (UI) and less than 10% of the 350ps setup time at 533 MT/s.

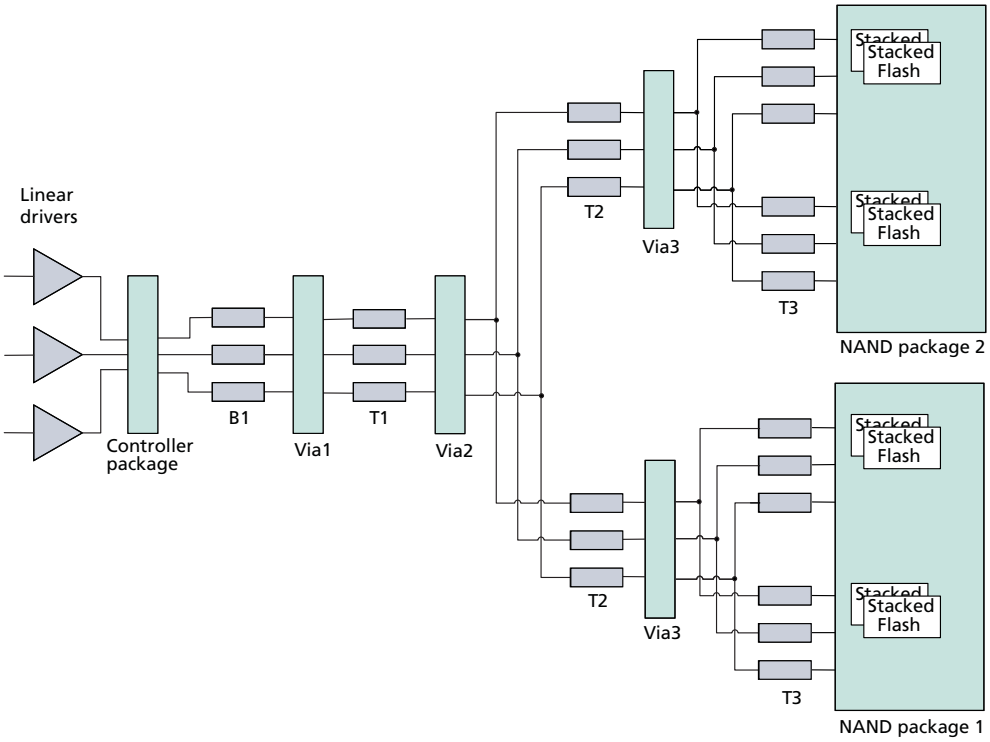
The guideline is ±0.1mm length matching among the Z_{Tline2} stubs. This is to control reflections and ringing especially for DQ reads. Failure to match the stub lengths results in waveform ripples. If stub matching is not feasible, the ripples can be damped by adding a series resistor.

SSD ODT and Drive Strength Guidelines

In developing SSD systems, some key considerations are the choices of the drive strengths and the on-die termination (ODT) values. These values vary from system to system and will depend on system host parameters including data rates, length of board transmission lines, number of dies, and length of package transmission lines. The drive strengths and ODT values have to be estimated by simulations and then verified through laboratory measurements. This section attempts to provide some guidelines to these choices based on simulations.

Figure 2 shows an SSD simulation deck schematic. For a single package configuration, there is no branching before T2. For the read configuration, the controller is the receiver, and the NAND die is the driver.

Figure 2: SSD System with Two NAND Packages in Write Topology



Varying Package Time Delay

Table 3 shows some of the simulation parameters for the SSD board. B1 and T3 are microstrip lines, and T1 and T2 are striplines. The trace widths on the board are 4 mils. The spacing between traces on the board is 4 mils on the microstrips, and 8 mils on the striplines.

Table 3: Simulation Parameters for SSD Board

Measurement	Component	Value	Unit
Length	B1	0.5	inch
	T1	4.5	
	T2	0.4	
	T3	0.4	
Capacitance	Via1	0.145	pF
	Via2	0.145	
	Via3	0.145	

Table 4 shows the estimated drive strengths and ODT values for an SSD system with two NAND packages by data rates, number of dies and package time delays. Each table entry denotes drive strength/ODT termination number. The ODT termination number can be decoded by using Table 5. Each table entry also associates with color shades, which indicates the risk severity of the system according to our signal integrity (SI) eye criteria. The area colored in white and no ODT termination number indicates that likely no ODT is required for the system. The area colored in light blue indicates lower risk and colored in dark blue indicates higher risk. The area colored in gray indicates no data is available which associates with the highest risk. Our SI eye criteria are based on the ONFI 4.0 setup, hold times, and the slew rate derating tables. The criteria are on the conservative side as the simulations are based on the worst case corners.

Table 4: Estimated Drive Strengths/ODT Values and T_d (SSD with Two NAND Packages)

System		System A		System B	
Number of Dies		8		12	
Package Time Delay T_d (ps)		37.1	99.0	37.1	99.0
Data Rate/Mode		**Drive Strengths/ODT Values**			
400 MT/s	Read	50/–	35/1	35/2	Note[3]
	Write	50/–	50/–	35/6	35/6
533 MT/s	Read	50/2	50/2	35/2	25/2
	Write	35/2	35/6	35/7	35/7
667 MT/s	Read	50/2	25/2	Note[3]	Note[3]
	Write	35/4	35/4	35/8	
800 MT/s	Read	35/4	Note[3]	Note[3]	
	Write	35/5			

Notes:
1. Each table entry denotes: drive strength/ODT termination number.
2. Shades of color indicates risk severity according to signal integrity eye criteria.
3. Difficult to implement due to highest risk according to signal integrity eye criteria.

Table 5: ODT Termination Number Decode

Termination Number	Resistance	Unit
1	150	Ohm
2	100	
3	75	
4	50	
5	37.5	
6	25	
7	18.75	
8	16.67	

Note: 1. Shades of color indicates higher risk severity according to signal integrity eye criteria.

The 12-die system has two NAND packages, with one package consists of 4 dies and another package consists of 8 dies. The result shown is the worse case between the receiver on the 4-die-package or the 8-die-package.

The packages are assumed to have 2 channels each. The system designers have to choose the appropriate dies to place the terminations based on their own implementations.

The following assumptions are made in the simulation:

- The package has I/O traces interleaved with power and ground traces.
- The wire bonding configuration is assumed to be flip-flop with all direct bonding and no cascade bonding.
- The power and ground traces have ideal voltages.
- The controller is simulated using a linear driver.
- C_{IO} is 1.5pF.
- The controller R_{ON} and ODT values have ±10% variation.

Table 6 shows the estimated drive strengths and ODT values for an SSD system with a single NAND package by data rates, number of dies, and package time delays.

Table 6: Estimated Drive Strengths/ODT Values and T_d (SDD with a Single NAND Package)

System		System A		System B	
Number of Dies		8		16	
Package Time Delay T_d (ps)		37.1	99.0	37.1	99.0
Data Rate/Mode		**Drive Strengths/ODT Values**			
400 MT/s	Read	50/–	35/1	35/2	25/2
	Write	50/–	50/–	18/6	35/6
533 MT/s	Read	50/2	50/2	35/2	35/4
	Write	50/–	50/–	25/7	35/5
667 MT/s	Read	50/2	50/2	Note[3]	
	Write	50/–	50/1		
800 MT/s	Read	50/2	25/2	Note[3]	
	Write	50/1	50/2		

Notes:
1. Each table entry denotes: drive strength/ODT termination number.
2. Shades of color indicates risk severity according to signal integrity eye criteria.
3. Difficult to implement due to highest risk according to signal integrity eye criteria.

The general trend is that higher data rates, larger number of dies, and longer package time delays require larger drive strengths and/or stronger ODT (that is less resistance).

It is difficult to implement 16 dies on a two-NAND-package system. It is more feasible to use a single NAND package with 16 dies. The results show that it may be challenging to achieve 667 MT/s or greater with 16 dies per channel even with the use of a single package.

Varying T1 Length

Table 7 shows some estimated drive strengths and ODT values for an SSD system with two NAND packages by data rates, number of dies, and different T1 lengths (Refer to Figure 2 regarding T1 position). The lengths of the other transmission lines are shown in Table 3.

Table 7: Estimated Drive Strengths/ODT Values and T1 Length (SSD with Two NAND Packages)

System		System A				System B			
Number of Dies		8				12			
T1 Length (inches)		1.00	2.25	4.50	7.00	1.00	2.25	4.50	7.00
Data Rate/Mode		**Drive Strengths/ODT Values**							
400 MT/s	Read	35/–	50/–	50/–	50/–	35/2	35/–	35/2	35/2
	Write	50/–	50/–	50/–	50/–	35/6	35/6	35/7	25/7
533 MT/s	Read	35/–	50/–	50/1	50/1	35/–	25/2	35/2	25/2
	Write	50/–	50/–	50/–	50/–	35/6	35/6	35/7	35/6
800 MT/s	Read	35/–	35/4	35/4	25/4	Note[3]			
	Write	35/3	50/4	35/5	25/4				

Notes:
1. Each table entry denotes: drive strength/ODT termination number.
2. Shades of color indicates risk severity according to signal integrity eye criteria.
3. Difficult to implement due to highest risk according to signal integrity eye criteria.

The first five assumptions made in the previous section are still valid for this data. In addition, the following are also assumed:

- The controller has a ±15% R_{ON} and ODT variation, instead of ±10% variation.
- The package time delay is 37.1ps.

Table 8 shows the drive strengths and ODT values for an SSD system with a single NAND package.

Table 8: Estimated Drive Strengths/ODT Values and T1 Length (SSD with a Single NAND Package)

System		System A				System B				System C			
Number of Dies		8				12				16			
T1 Length (inches)		1.00	2.25	4.50	7.00	1.00	2.25	4.50	7.00	1.00	2.25	4.50	7.00
Data Rate/Mode		**Drive Strengths/ODT Values**											
400 MT/s	Read	50/–	50/–	50/–	50/–	50/–	50/–	50/2	50/2	35/–	50/–	35/2	35/2
	Write	50/–	50/–	50/–	50/–	50/–	50/–	50/–	35/3	18/1	18/5	18/6	18/6
533 MT/s	Read	50/–	50/–	50/2	50/2	50/–	50/2	50/2	50/2	50/–	35/2	35/2	35/2
	Write	50/–	50/–	50/–	50/–	35/–	35/–	35/6	35/5	25/3	25/5	25/7	25/7
667 MT/s	Read	50/2	50/2	50/2	50/2	35/2	50/2	35/2	35/2	Note[3]			
	Write	50/–	50/–	50/–	50/1	35/2	35/3	35/4	35/5				
800 MT/s	Read	50/2	50/2	50/2	35/2	Note[3]				Note[3]			
	Write	50/–	50/1	50/1	35/1								

Notes:
1. Each table entry denotes: drive strength/ODT termination number.
2. Shades of color indicates risk severity according to signal integrity eye criteria.
3. Difficult to implement due to highest risk according to signal integrity eye criteria.

The general trend is that longer channels, larger number of die, and higher data rates require larger drive strengths and/or stronger ODT (that is less resistance).

Conclusion

This technical note presents some new features in ONFI 4.0 from a signaling perspective. This technical note also provides design guidelines for tree topology, and discusses the tolerance of the main transmission line and the length matching between stubs. In addition, this technical note provides guidelines on drive strengths and ODT values for SSD systems with a single NAND package and with two NAND packages based on simulation data. The end users are expected to perform system simulations and conduct laboratory measurements to verify their system designs.

Revision History

Rev. A– 12/15

- Initial release

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