A 512Gb 3-bit/Cell 7th-Generation 3D NAND Flash Memory with 184MB/s Write Throughput and 2.0Gb/s Interface


Samsung Electronics, South Korea
Self Introduction

Education Background

• B.S degree in Computer Science Engineering from Pusan National University, Pusan, South Korea, in 1998

Work Experience

• Have been with Samsung Electronics since 1998
• Designed Planar NOR/NAND Flash 1998-2012
• Designed VNAND [2\textsuperscript{nd} / 4\textsuperscript{th} / 7\textsuperscript{th} Gen.] since 2013 as Project Leader

Research Interest

• Memory Architecture / Circuit Design Cell Characteristic / Fault Analysis
• Business Strategy / Applications of Memory

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Technologies for 7th Generation 3D-NAND

Performance

• Conventional BL Forcing
• 2-step BL Forcing w/Dynamic latch
• 2-step BL/WL Forcing

Power Consumption for COP Architecture

• MIM Cap for COP
• Optimization of Pumping Capacitors

2.0Gbps IO Support

• Dual Interface of Termination type
Conventional BL Forcing

With BL forcing, the programming electric field between SEL WL and Channel is reduced.
2-step BL forcing w/Dynamic latch

*Two-step BL Forcing

Forcing Region1 (Vforc1)  Forcing Region2 (Vforc2)

Normal Cell Region

1step  2step  Internal Forcing

Concept of *TBF

Forcing Step1 & 2=> Upper Control

Timing Diagram of TBF

Dynamic Latch with TBF

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2-step BL/WL forcing

*Two-step BL/WL Forcing

Concept of *TBWF

Timing Diagram of TBWF

Forcing Step1 => Upper Control
Forcing Step2 => Under Control
Comparison of pumping capacitors of 3D NAND

Pumping capacitors of metal contact is not available in Cell Over Peri Architecture. So, power and area efficiency of charge pumps is degraded.
1\textsuperscript{st} Stage LVN Cap. & MIM Cap for COP

Optimization of pumping capacitors by series stage

1\textsuperscript{st} Stage LVN Cap. & MIM caps for COP achieve 24\% power reduction and 27\% area reduction of charge pumps
Toggle 4.0 Interface

For high speed SI, using strong ODT is required. But it increases channel power consumption.

Driver & ODT

CTT Interface Signaling

VOH = VccQ
VOL = VSS

w/o ODT

w/ Rtt1

w/ Rtt2

Driver

ODT

Transmission Line

Ron#

Rtt#

Rtt#
## Dual Interface

<table>
<thead>
<tr>
<th>Interface Type</th>
<th>(A) CTT</th>
<th>(B) LTT</th>
<th>(C) V-NAND 7th Gen (Dual interface)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit Topology</td>
<td><img src="image1.png" alt="CTT Circuit" /></td>
<td><img src="image2.png" alt="LTT Circuit" /></td>
<td><img src="image3.png" alt="V-NAND Circuit" /></td>
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<tr>
<td>Signaling</td>
<td><img src="image4.png" alt="CTT Signaling" /></td>
<td><img src="image5.png" alt="LTT Signaling" /></td>
<td><img src="image6.png" alt="V-NAND Signaling" /></td>
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<tr>
<td>Tr. type</td>
<td>CTT mode</td>
<td>LTT mode</td>
<td></td>
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<tr>
<td>Pull Up</td>
<td>PMOS</td>
<td>NMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td>Pull Down</td>
<td>NMOS</td>
<td>NMOS</td>
<td>NMOS</td>
</tr>
</tbody>
</table>

**Comparison of Interface type**

Dual Interface: In heavy load systems, select CTT interface mode and in lighter-load systems select LTT interface mode.
Power comparison

At 2Gbps I/O speed, 62% channel power reduction in LTT interface than in CTT interface.
Conclusion - 7th Generation 512Gb 3D NAND

### Feature Summary

<table>
<thead>
<tr>
<th></th>
<th>ISSCC 2019[1]</th>
<th>This Work</th>
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<tbody>
<tr>
<td>Bits per cell</td>
<td>3</td>
<td>3</td>
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<tr>
<td>Density</td>
<td>512Gb</td>
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<tr>
<td>Page Size</td>
<td>16KB/Page</td>
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<tr>
<td>Bit Density</td>
<td>5Gb/mm²</td>
<td>8.5Gb/mm²</td>
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<tr>
<td>I/O Bandwidth</td>
<td>Max. 1.2Gb/s</td>
<td>Max. 2.0Gb/s</td>
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<td>tBERS</td>
<td>3.5ms (Typ.)</td>
<td>3.5ms (Typ.)</td>
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<td>tR</td>
<td>45us</td>
<td>40us</td>
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<td>Program Throughput</td>
<td>82MB/s</td>
<td>184MB/s</td>
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<tr>
<td>Vcc</td>
<td>2.35V to 3.6V</td>
<td>2.35V to 3.6V</td>
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<tr>
<td>Vccq</td>
<td>1.2V</td>
<td>1.2V</td>
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